CS 4341  
Fall 2017  
Homework #4

Assigned: October 17, 2017

Due: October 27, 2017

Objective:

Complete the following Exercises. They are from the Dally book. For the written Exercises and diagrams, students are expected to turn in digital forms or scans into the Blackboard system as a zip file for their cohort.

This homework has 2 main sections:

* Factoring a State Machine (30 points)
* Verilog of a Factored State Machine (25 points)
* Solving contamination and propagation delays without flip-flops (20 points)
* Solving contamination and propagation delays with flip-flops (25 points)

Special Notice 1:

Turn in Homework 4 as a zip file, in the form of hw4.cohortname.zip. Your cohort name and class section must be at the top of each file. If the assignment is not turned in correctly, the teaching assistants are allowed to deduct 25 points for “Lack of Effort”

Special Notice 2:

If you use additional software to solve the homework, you will need to cite the software in proper format including the publication information about the software.

Special Notice 3:

If you “over-engineer” the answer to a problem, and the resulting diagram and code is so different that the answer cannot be readily recognized, full points will be deducted for that problem. This means that your answers ***must have labels***. Turning in a state machine with no labels or appropriate definitions will not be accepted.

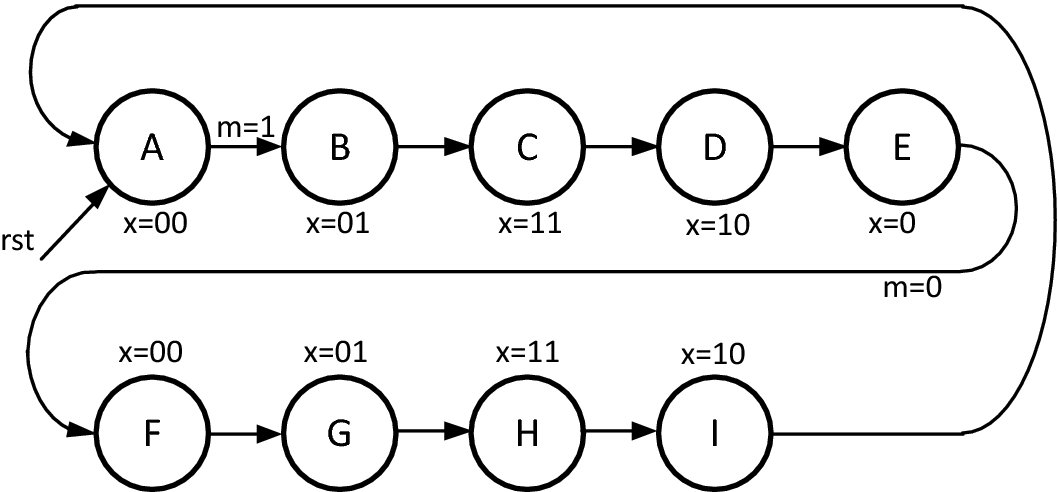


Figure 17.17

17.1 Factor a state Diagram I-I. Consider the state diagram shown in figure 17.17.

*Note: Look at the counters and timers and the sequence involved to get a hint of how to solve the problem. You will need to add in transitions between the two state machines.*

1. Identify identical or nearly identical states in this FSM (10 marks)
2. Draw the state diagram for a separate FSM that implements these sequences of states-inputs should select between variations in the sequence. (10 marks)
3. Draw a revised top-level state diagram that invokes your FSM from (b) to implement the repeated sequence. (10 Marks)

17.1 Additional

The assignment is to FACTOR a finite state machine. DO NOT REDUCE the finite state machine.

How many states should the control state machine be? How many rows are in the diagram? Look back at the flashing light example in the slides or the text.

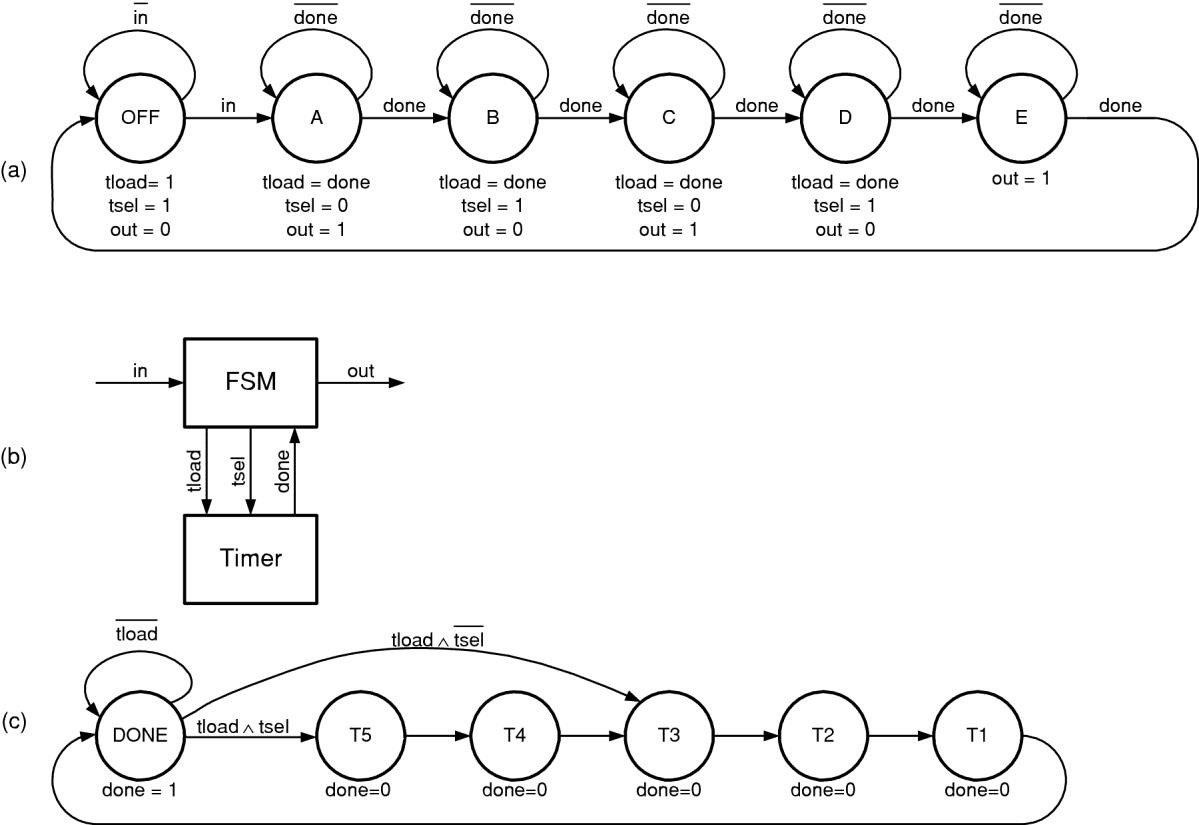
State E has x=0. Dr. Becker considers this to be a typo, or a lame hint about machine structure. X will equal 00 in state E.

The state machine will be broken into multiple parts based on the identical components. Look at the value of x to determine if there is a pattern.

Yes, one sequence starts x=00, and the other sequence starts x=00,x=00. Again, see the flashing light example for an idea on how to handle this.

Top Level Diagram

There will be two state machines, one to control the commands, the other to handle the data sequence (x). Like figure 17.2



17.2 Factor a state diagram, I-II. Implement your factored state machine from Exercise 17.1 in Verilog. (25 Marks)

17.2 Additional

For the Verilog, you will need to program the multiple state machines to show their equivalence.

Example Output: Dr. Becker’s version compares the original state machine to the factored state machine. CRM is Clock, Reset, and M-Transition. The first X column is the original state machine output. The second X column is the Factored State Machines output. The outputs are then compared in Match.

C:\iverilog\workspace>vvp a.out

CRM||State| x||Control|Sel|Go|| FXX| x|rdy|Match

---++-----+---++-------+---+--++-----+--+---+-----

**000|**| xxxx| **xx|**| xx| x| x||xxxxx|**xx|** x|**x**

**110|**| xxxx| **xx|**| xx| x| x||xxxxx|**xx|** x|**x**

**010|**| 0000| **00|**| 01| 1| 0||00001|**00|** 1|**1**

**101|**| 0000| **00|**| 01| 1| 0||00001|**00|** 1|**1**

**001|**| 0000| **00|**| 01| 1| 1||00001|**00|** 1|**1**

**101|**| 0000| **00|**| 01| 1| 1||00001|**00|** 1|**1**

**001|**| 0001| **01|**| 10| 0| 0||00100|**01|** 0|**1**

**101|**| 0001| **01|**| 10| 0| 0||00100|**01|** 0|**1**

**001|**| 0010| **11|**| 10| 0| 0||01000|**11|** 0|**1**

**101|**| 0010| **11|**| 10| 0| 0||01000|**11|** 0|**1**

**001|**| 0011| **10|**| 10| 0| 0||10000|**10|** 0|**1**

**101|**| 0011| **10|**| 10| 0| 0||10000|**10|** 0|**1**

**001|**| 0101| **00|**| 10| 0| 0||00001|**00|** 1|**1**

**101|**| 0101| **00|**| 10| 0| 0||00001|**00|** 1|**1**

**001|**| 0101| **00|**| 10| 0| 0||00001|**00|** 1|**1**

**101|**| 0101| **00|**| 10| 0| 0||00001|**00|** 1|**1**

**001|**| 0101| **00|**| 10| 0| 0||00001|**00|** 1|**1**

**101|**| 0101| **00|**| 10| 0| 0||00001|**00|** 1|**1**

**001|**| 0101| **00|**| 10| 0| 0||00001|**00|** 1|**1**

**100|**| 0101| **00|**| 10| 0| 0||00001|**00|** 1|**1**

**000|**| 0101| **00|**| 10| 0| 1||00001|**00|** 1|**1**

**100|**| 0101| **00|**| 10| 0| 1||00001|**00|** 1|**1**

**000|**| 1000| **00|**| 01| 1| 0||00010|**00|** 0|**1**

**100|**| 1000| **00|**| 01| 1| 0||00010|**00|** 0|**1**

**000|**| 1001| **01|**| 01| 1| 0||00100|**01|** 0|**1**

**100|**| 1001| **01|**| 01| 1| 0||00100|**01|** 0|**1**

**000|**| 1010| **11|**| 01| 1| 0||01000|**11|** 0|**1**

**100|**| 1010| **11|**| 01| 1| 0||01000|**11|** 0|**1**

**000|**| 1011| **10|**| 01| 1| 0||10000|**10|** 0|**1**

**100|**| 1011| **10|**| 01| 1| 0||10000|**10|** 0|**1**

**000|**| 0000| **00|**| 01| 1| 0||00001|**00|** 1|**1**

**100|**| 0000| **00|**| 01| 1| 0||00001|**00|** 1|**1**

**000|**| 0000| **00|**| 01| 1| 0||00001|**00|** 1|**1**

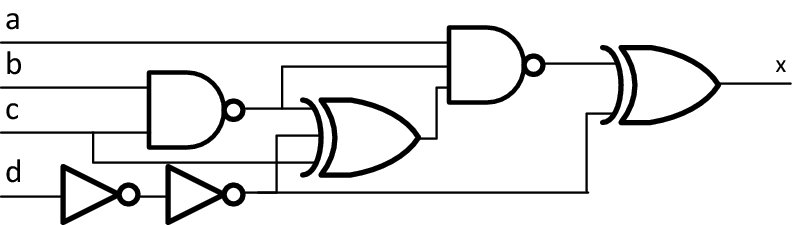


Figure 15.17

15.1 Propagation and contamination delays, I. Calculate the propagation and contamination delays of each input to the output in Figure 15.17. Assume that each gate has a 10 ps delay. (20 marks)

*Note: You will need to show the delays for all four inputs: a,b,c,d. This problem has 4 answers.*

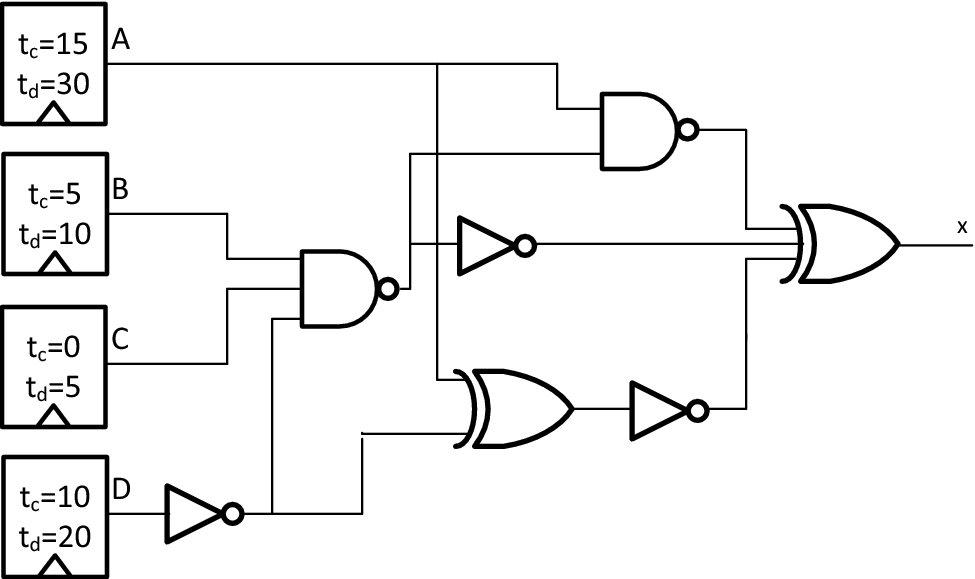


Figure 15.18

15.2 Propagation and contamination delays II. Compute the contamination and propagation delays of the circuit in figure 15.18 from flip-flop A to the output. Assume that the delay through each gate is 10 ps. (5 marks)

15.3 Propagation and contamination delays III. Compute the contamination and propagation delays of the circuit in figure 15.18 from flip-flop B to the output. Assume that the delay through each gate is 10 ps. (5 marks)

15.4 Propagation and contamination delays IV. Compute the contamination and propagation delays of the circuit in figure 15.18 from flip-flop C to the output. Assume that the delay through each gate is 10 ps. (5 marks)

15.5 Propagation and contamination delays V. Compute the contamination and propagation delays of the circuit in figure 15.18 from flip-flop D to the output. Assume that the delay through each gate is 10 ps. (5 marks)

15.6 Propagation and contamination delays VI. What are the overall contamination and propagation delays of the circuit in figure 15.18? Assume the delay through each gate is 10 ps. (5 marks)

*Note: The overall contamination delay is the minimum contamination delay over all paths. The Overall propagation delay is the maximum propagation delay over all paths.*